FAIRCHILD SEMICONDUCTOR®

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74ABT16245
16-Bit Transceiver with 3-STATE Outputs

General Description

The ABT16245 contains sixteen non-inverting bidirectional buffers with 3-STATE outputs and is intended for bus oriented applications. The device is byte controlled. Each byte has separate control inputs which can be shorted together for full 16-bit operation. The T/$\overline{R}$ inputs determine the direction of data flow through the device. The $\overline{OE}$ inputs disable both the A and B ports by placing them in a high impedance state.

Features

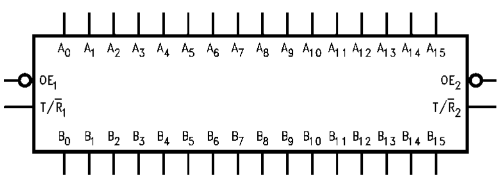
- Bidirectional non-inverting buffers
- Separate control logic for each byte
- 16-bit version of the ABT245
- A and B output sink capability of 64 mA, source capability of 32 mA
- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Output switching specified for both 50 pF and 250 pF loads
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Non-destructive hot insertion capability

Ordering Code:

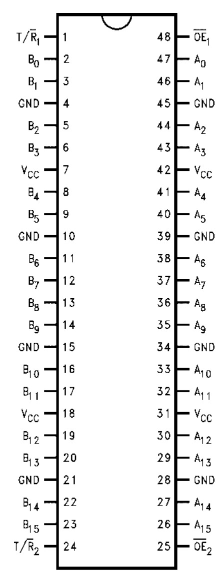
Order Number	Package Number	Package Description
74ABT16245CSSC	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
74ABT16245CMTD	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter “X” to the ordering code.

Logic Symbol



Connection Diagram



Pin Descriptions

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active LOW)
T/$\overline{R}_n$	Transmit/Receive Input
A_0–A_{15}	Side A Inputs/Outputs
B_0–B_{15}	Side B Inputs/Outputs

Truth Tables

Inputs		Outputs
$\overline{OE_1}$	$T/\overline{R_1}$	
L	L	Bus B_0–B_7 Data to Bus A_0–A_7
L	H	Bus A_0–A_7 Data to Bus B_0–B_7
H	X	HIGH-Z State on A_0–A_7, B_0–B_7

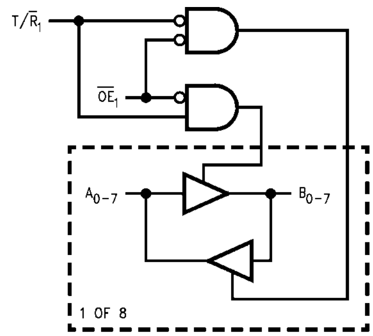
Inputs		Outputs
$\overline{OE_2}$	$T/\overline{R_2}$	
L	L	Bus B_8–B_{15} Data to Bus A_8–A_{15}
L	H	Bus A_8–A_{15} Data to Bus B_8–B_{15}
H	X	HIGH-Z State on A_8–A_{15}, B_8–B_{15}

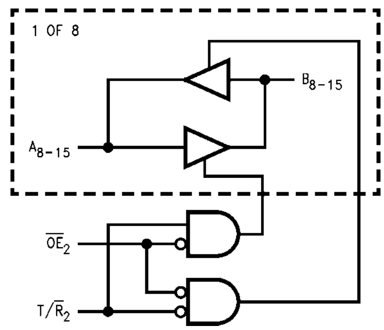
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Functional Description

The ABT16245 contains sixteen non-inverting bidirectional buffers with 3-STATE outputs. The device is byte controlled with each byte functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation.

Logic Diagrams





Absolute Maximum Ratings(Note 1)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output	
in the Disabled or	
Power-Off State	−0.5V to 5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output	
in LOW State (Max)	twice the rated I_{OL} (mA)
DC Latchup Source Current	−500 mA
Over Voltage Latchup (I/O)	10V

Recommended Operating Conditions

Free Air Ambient Temperature	−40°C to +85°C
Supply Voltage	+4.5V to +5.5V
Minimum Input Edge Rate (ΔV/Δt)	
Data Input	50 mV/ns
Enable Input	20 mV/ns

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage			0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I_{IN} = −18 mA ($\overline{OE}_n$, T/$\overline{R}_n$)
V_{OH}	Output HIGH Voltage	2.5			V	Min	I_{OH} = −3 mA (A_n, B_n)
		2.0			V	Min	I_{OH} = −32 mA (A_n, B_n)
V_{OL}	Output LOW Voltage			0.55	V	Min	I_{OL} = 64 mA (A_n, B_n)
I_{IH}	Input HIGH Current			1 1	μA	Max	V_{IN} = 2.7V ($\overline{OE}_n$, T/$\overline{R}_n$) (Note 3) V_{IN} = V_{CC} ($\overline{OE}_n$, T/$\overline{R}_n$)
I_{BVI}	Input HIGH Current Breakdown Test			7	μA	Max	V_{IN} = 7.0V ($\overline{OE}_n$, T/$\overline{R}_n$)
I_{BVIT}	Input HIGH Current Breakdown Test (I/O)			100	μA	Max	V_{IN} = 5.5V (A_n, B_n)
I_{IL}	Input LOW Current			−1 −1	μA	Max	V_{IN} = 0.5V ($\overline{OE}_n$, T/$\overline{R}_n$) (Note 3) V_{IN} = 0.0V ($\overline{OE}_n$, T/$\overline{R}_n$)
V_{ID}	Input Leakage Test	4.75			V	0.0	I_{ID} = 1.9 μA ($\overline{OE}_n$, T/$\overline{R}_n$) All Other Pins Grounded
I_{IH} + I_{OZH}	Output Leakage Current			10	μA	0 − 5.5V	V_{OUT} = 2.7V (A_n, B_n); $\overline{OE}$ = 2.0V
I_{IL} + I_{OZL}	Output Leakage Current			−10	μA	0 − 5.5V	V_{OUT} = 0.5V (A_n, B_n); $\overline{OE}$ = 2.0V
I_{OS}	Output Short-Circuit Current	−100		−275	mA	Max	V_{OUT} = 0.0V (A_n, B_n)
I_{CEX}	Output HIGH Leakage Current			50	μA	Max	V_{OUT} = V_{CC} (A_n, B_n)
I_{ZZ}	Bus Drainage Test			100	μA	0.0	V_{OUT} = 5.50V (A_n, B_n); All Others GND
I_{CCH}	Power Supply Current			100	μA	Max	All Outputs HIGH
I_{CCL}	Power Supply Current			60	mA	Max	All Outputs LOW
I_{CCZ}	Power Supply Current			100	μA	Max	$\overline{OE}_n$ = V_{CC}, T/$\overline{R}_n$ = GND or V_{CC} All others at V_{CC} or GND
I_{CCT}	Additional I_{CC}/Input: Outputs Enabled Outputs 3-STATE Outputs 3-STATE			2.5 2.5 50	mA mA μA	Max	V_I = V_{CC} − 2.1V $\overline{OE}_n$, T/$\overline{R}_n$ V_I = V_{CC} − 2.1V Data Input V_I = V_{CC} − 2.1V All others at V_{CC} or GND
I_{CCD}	Dynamic I_{CC} (Note 3) No Load			0.1	mA/ MHz	Max	Outputs OPEN $\overline{OE}_n$ = GND, T/$\overline{R}_n$ = GND or V_{CC} One Bit Toggling, 50% Duty Cycle

Note 3: Guaranteed, but not tested.

DC Extended Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Units	V_{CC}	Conditions $C_L = 50$ pF; $R_L = 500\Omega$
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}		0.5	0.9	V	5.0	$T_A = 25°C$ (Note 4)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	−1.4	−1.0		V	5.0	$T_A = 25°C$ (Note 4)
V_{OHV}	Minimum HIGH Level Dynamic Output Voltage	2.5	3.0		V	5.0	$T_A = 25°C$ (Note 5)
V_{IHD}	Minimum HIGH Level Dynamic Input Voltage	2.0	1.4		V	5.0	$T_A = 25°C$ (Note 5)
V_{ILD}	Maximum LOW Level Dynamic Input Voltage		1.2	0.8	V	5.0	$T_A = 25°C$ (Note 6)

Note 4: Max number of outputs defined as (n). n – 1 data inputs are driven 0V to 3V. One output at LOW. Guaranteed, but not tested.

Note 5: Max number of outputs defined as (n). n – 1 data inputs are driven 0V to 3V. One output HIGH. Guaranteed, but not tested.

Note 6: Max number of data inputs (n) switching. n – 1 inputs switching 0V to 3V. Input-under-test switching: 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}). Guaranteed, but not tested.

AC Electrical Characteristics

Symbol	Parameter	$T_A = +25°C$, $V_{CC} = +5V$, $C_L = 50$ pF			$T_A = -55°C$ to $+125°C$, $V_{CC} = 4.5V – 5.5V$, $C_L = 50$ pF		$T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V – 5.5V$, $C_L = 50$ pF		Units
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}	Propagation	1.0	2.4	3.9	0.5	4.5	1.0	3.9	ns
t_{PHL}	Delay Data to Outputs	1.0	2.8	3.9	0.5	5.2	1.0	3.9	
t_{PZH}	Output Enable	1.5	3.6	6.3	0.8	6.4	1.5	6.3	ns
t_{PZL}	Time	1.5	3.7	6.3	0.9	6.9	1.5	6.3	
t_{PHZ}	Output Disable	1.3	4.6	6.9	1.3	6.9	1.3	6.9	ns
t_{PLZ}	Time	1.3	3.7	6.9	1.0	6.9	1.3	6.9	

Extended AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V–5.5V$, $C_L = 50$ pF, 16 Outputs Switching (Note 7)			$T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V–5.5V$, $C_L = 250$ pF, 1 Output Switching (Note 8)		$T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V–5.5V$, $C_L = 250$ pF, 16 Outputs Switching (Note 9)		Units
		Min	Typ	Max	Min	Max	Min	Max	
f_{TOGGLE}	Maximum Toggle Frequency		100						MHz
t_{PLH}	Propagation Delay	1.5		5.0	1.5	6.0	2.5	8.0	ns
t_{PHL}	Data to Outputs	1.5		5.3	1.5	6.0	2.5	8.0	
t_{PZH}	Output Enable	1.5		6.5	2.5	8.2	2.5	10.0	ns
t_{PZL}	Time	1.5		6.5	2.5	8.2	2.5	9.0	
t_{PHZ}	Output Disable	1.0		6.9	(Note 10)		(Note 10)		ns
t_{PLZ}	Time	1.0		6.9					

Note 7: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.).

Note 8: This specification is guaranteed but not tested. The limits represent propagation delay with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Note 9: This specification is guaranteed but not tested. The limits represent propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.) with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

Note 10: 3-STATE delay are dominated by the RC network (500Ω, 250 pF) on the output and have been excluded from the datasheet.

Skew

Symbol	Parameter	$T_A = -40°C$ to $+85°C$ $V_{CC} = 4.5V–5.5V$ $C_L = 50$ pF 16 Outputs Switching (Note 11)	$T_A = -40°C$ to $+85°C$ $V_{CC} = 4.5V–5.5V$ $C_L = 250$ pF 16 Outputs Switching (Note 12)	Units
		Max	Max	
t_{OSHL} (Note 13)	Pin to Pin Skew HL Transitions	1.3	1.5	ns
t_{OSLH} (Note 13)	Pin to Pin Skew LH Transitions	1.3	1.5	ns
t_{PS} (Note 14)	Duty Cycle LH–HL Skew	1.5	2.0	ns
t_{OST} (Note 13)	Pin to Pin Skew LH/HL Transitions	1.7	2.5	ns
t_{PV} (Note 15)	Device to Device Skew LH/HL Transitions	2.0	3.0	ns

Note 11: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.)

Note 12: These specifications guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

Note 13: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW (t_{OSHL}), LOW to HIGH (t_{OSLH}), or any combination switching LOW-to-HIGH and/or HIGH-to-LOW (t_{OST}). The specification is guaranteed but not tested.

Note 14: This describes the difference between the delay of the LOW-to-HIGH and the HIGH-to-LOW transition on the same pin. It is measured across all the outputs (drivers) on the same chip, the worst (largest delta) number is the guaranteed specification. This specification is guaranteed but not tested.

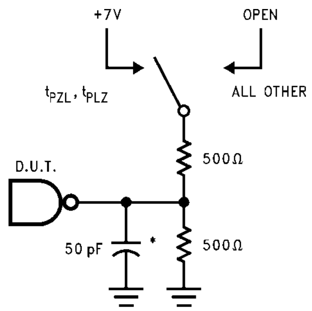
Note 15: Propagation delay variation for a given set of conditions (i.e., temperature and V_{CC}) from device to device. This specification is guaranteed but not tested.

Capacitance

Symbol	Parameter	Typ	Units	Conditions $T_A = 25°C$
C_{IN}	Input Capacitance	5	pF	$V_{CC} = 0.0V$ ($\overline{OE}_n$, $T/\overline{R}_n$)
$C_{I/O}$ (Note 16)	Output Capacitance	11	pF	$V_{CC} = 5.0V$ (A_n, B_n)

Note 16: $C_{I/O}$ is measured at frequency f = 1 MHz, per MIL-STD-883, Method 3012.

AC Loading



*Includes jig and probe capacitance

FIGURE 1. Standard AC Test Load

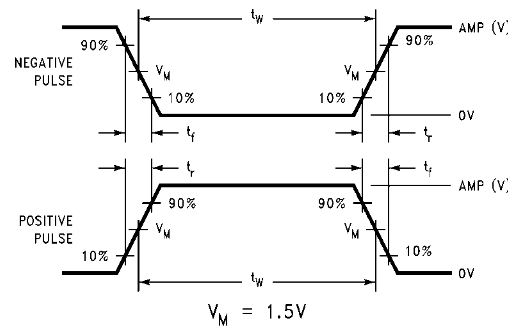


FIGURE 2. Input Pulse Requirements

Amplitude	Rep. Rate	t_W	t_r	t_f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 3. Test Input Signal Requirements

AC Waveforms

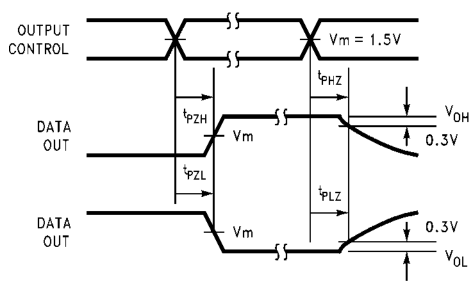


FIGURE 4. 3-STATE Output HIGH and LOW Enable and Disable Times

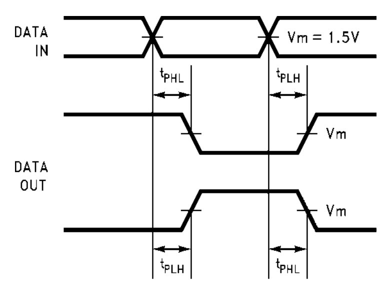


FIGURE 6. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

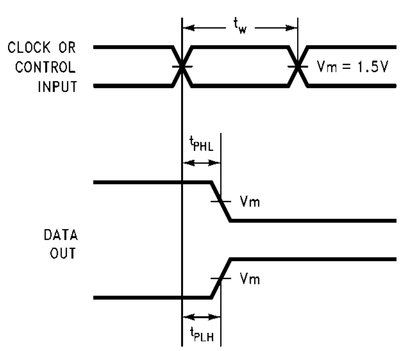


FIGURE 5. Propagation Delay, Pulse Width Waveforms

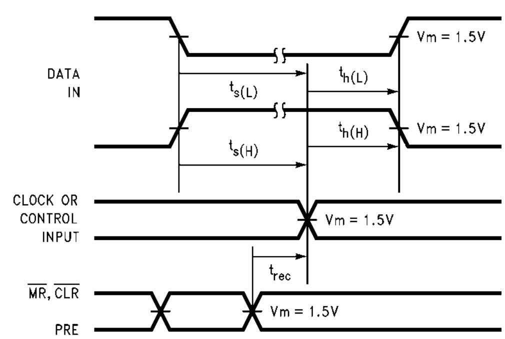
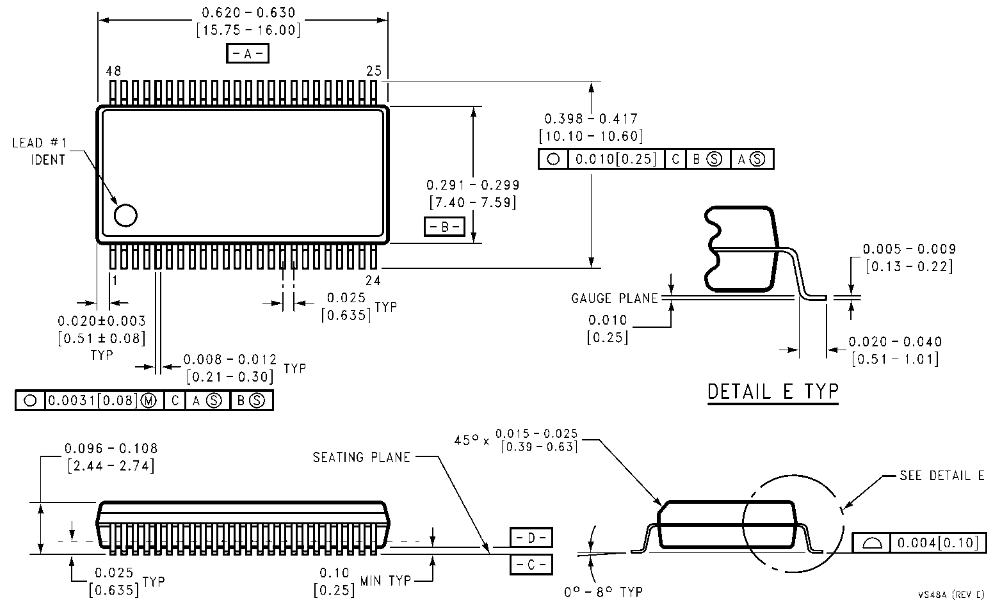


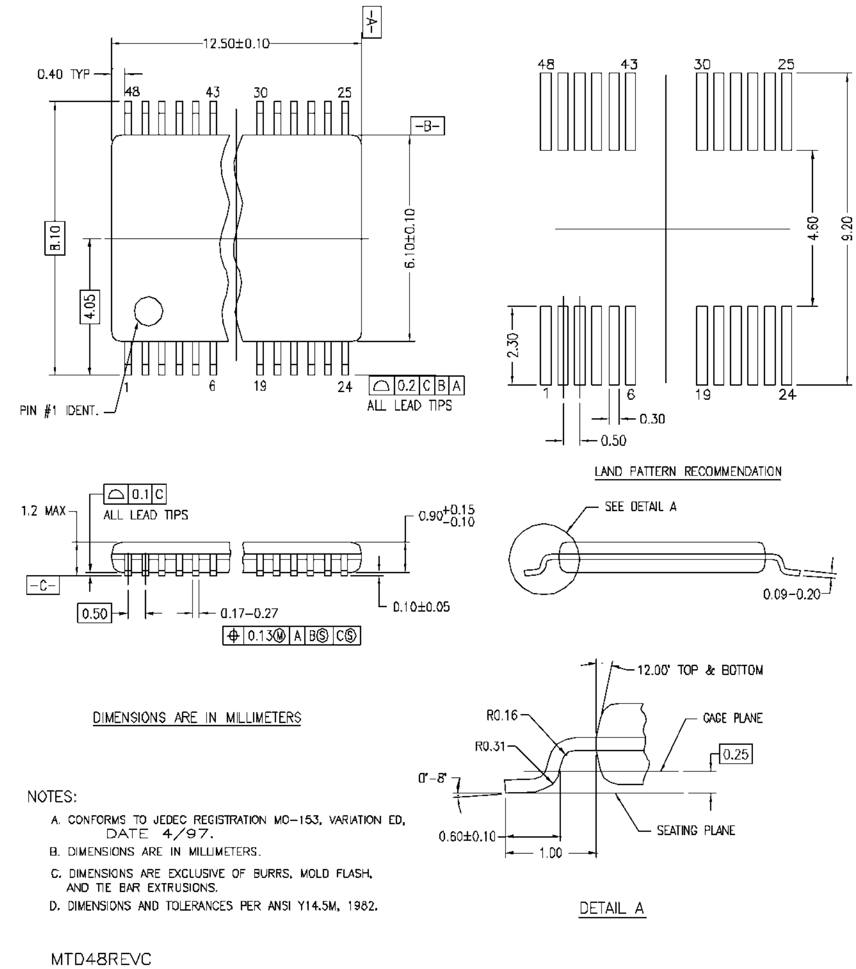
FIGURE 7. Setup Time, Hold Time and Recovery Time Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted



48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
Package Number MS48A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD48